IN THE CLAIMS:

Please cancel claims 16 and 20 in their entirety without prejudice nor disclaimer of the subject matter set forth therein.

Please amend claims 1, 18 and 21-24 and add new claims 25-28 as follows.

1. (Currently Amended) A semiconductor device comprising:

a lower electrode formed on a substrate;

a capacitive insulating film made of a ferroelectric film on the lower electrode;

an upper electrode formed on the capacitive insulating film; ~~and~~

a contact layer formed directly on the upper electrode so as not to be in contact with the capacitive insulating film;

an insulating film made of silicon dioxide or nitride formed directly on the contact layer to cover the lower electrode, the capacitive insulating film, the upper electrode and the contact layer, and

wherein the contact layer is provided on a surface of the upper electrode and in a region other than the region where a metal interconnect is connected to the upper electrode, and

wherein the contact layer is a single layer film or a multilayer structure, the single-layer film being made of a metal oxide or a metal nitride, the multilayer structure being made up of metal oxide and metal nitride films.

2. (Cancelled).

3. (Withdrawn) A method for fabricating a semiconductor device, comprising the steps of:

a) depositing a first metal film, a ferroelectric film, a second metal film and a single-layer film or a multilayer structure in this order on a substrate, the single-layer film being made of a metal oxide or a metal nitride, the multilayer structure being made up of metal oxide and metal nitride films;

b) patterning the single-layer film or the multilayer structure to form a contact layer;

c) patterning the second metal film to form an upper electrode;

d) patterning the ferroelectric film to form a capacitive insulating film;

e) patterning the first metal film to form a lower electrode;

f) depositing an insulating film covering the lower electrode, the capacitive insulating film, the upper electrode and the contact layer;

g) opening a contact hole that passes through the insulating film and the contact layer to reach the upper electrode; and

h) defining a metal interconnect, which is filled in the contact hole and connected to the upper electrode, on a part of the insulating film.

4. (Withdrawn) The device of Claim 3, wherein in the step a), the single-layer film or the multilayer structure is deposited by a sputtering process using a target of a metal oxide or a metal nitride or by a reactive sputtering process performed within an ambient containing oxygen gas or nitrogen gas.

5. (Withdrawn) The method of Claim 3, further comprising the step of annealing the second metal film at a temperature between 300°C and 800°C.

6-9. (Cancelled).

10. (Previously Amended) The device of Claim 1,

wherein the metal oxide film is made of an oxide of Ti or an oxide of Ta, while the metal nitride film is made of a nitride of Ti or a nitride of Ta.

11-12. (Cancelled).

13. (Previously presented) The device of Claim 1, wherein the ferroelectric film includes $SrBi_2Ta_2O_9$.

14. (Previously presented) The device of Claim 1, wherein the insulating film is unlikely to peel off due to the contact layer.

15. (Previously presented) The device of Claim 1, wherein the contact layer is made from metal atoms which are unlikely to diffuse into the upper electrode.

16. (Canceled)

17. (Previously Presented) The device of Claim 1, wherein a portion of the upper surface of the upper electrode is not covered by the contact layer and connected to the metal interconnect.

18. (Currently Amended) A semiconductor device comprising:

a lower electrode formed on a substrate;

a capacitive insulating film made of a ferroelectric film on the lower electrode;

an upper electrode formed on the capacitive insulating film; ~~and~~

a contact layer formed directly on the upper electrode so as to be in no contact with the capacitive insulating film, and

an insulating film made of silicon dioxide or nitride formed directly on the contact layer to cover the lower electrode, the capacitive insulating film, the upper electrode and the contact layer,

wherein a portion of the upper surface of the upper electrode is not covered by the contact layer and connected to a metal interconnect, and

wherein the contact layer is a single-layer film or a multilayer structure, the single-layer film being made of a metal oxide or a metal nitride, the multilayer structure being made up of metal oxide ~~film~~ and metal nitride films.

19. (Previously Presented) The device of Claim 18, wherein the metal oxide film is made of an oxide of Ti or an oxide of Ta, while the metal nitride film is made of a nitride of Ti or a nitride of Ta.

20. (Canceled)

21. (Currently Amended) A semiconductor device comprising:

a lower electrode formed on a substrate;

a capacitive insulating film made of a ferroelectric film on the lower electrode;

an upper electrode formed on the capacitive insulating film;

a contact layer formed directly on the upper electrode so as to be in no contact with the capacitive insulating film; and

an insulating film formed directly on the contact layer so as to cover the lower electrode, the capacitive insulating film and the upper electrode, and the insulating film being connected to the lower electrode and/or the capacitive insulating film,

wherein the entire upper surface of the upper electrode is in no contact with the insulating film, and

wherein the contact layer is a single-layer film or a multilayer structure, the single-layer film being made of a metal oxide or metal nitride, the multilayer structure being made up of metal oxide films and metal nitride films, and

wherein a portion of the upper surface of the capacitive insulating film is covered by the insulating film.

22. (Currently Amended) The device of Claim 21, wherein the metal oxide film is made of an oxide of Ti or an oxide of Ta, while the metal nitride film is made of a nitride of Ti or a nitride of Ta.

23. (Currently Amended) A semiconductor device comprising:

a lower electrode ~~form~~ formed on a substrate;

a capacitive insulating film made of a ferroelectric film on the lower electrode,

an upper electrode formed on the capacitive insulating film; and

a contact layer formed directly on the upper electrode so as to be in no contact with the capacitive insulating film,

wherein the entire upper surface of the upper electrode is in no contact with an insulating film, and

wherein the contact layer is made from TaO or TaN.

24. (Currently Amended) A semiconductor device comprising;

a capacitor formed on a substrate and ~~the~~ including a lower electrode, a capacitive insulating film of a ferroelectric film and an upper electrode; and

a contact layer formed directly on the upper electrode so as to be in no contact with the capacitive insulating film,

wherein the entire upper surface of the upper electrode is in no contact with an insulating film which is formed directly on the contact layer, so as to cover the capacitor ~~deviee~~, and in contact with the lower electrode and/or the capacitive insulating film, and

wherein the contact layer is a single-layer film or a multilayer structure, the single-layer film being made of a metal oxide or a metal nitride, the multilayer structure being made up of metal oxide ~~films~~ and metal nitride films, and

wherein a portion of the upper surface of the capacitive insulating film is covered by the insulating film.

25. (New) The device of Claim 1, wherein a portion of the upper surface of the capacitive insulating film is covered by the insulating film.

26. (New) The device of Claim 18, wherein a portion of the upper surface of the capacitive insulating film is covered by the insulating film.

27. (New) The device of Claim 21, wherein the contact layer is provided on a surface of the upper electrode and in a region other than the region where a metal interconnect is connected to the upper electrode.

28. (New) The device of Claim 24, wherein the contact layer is provided on a surface of the upper electrode and in a region other than the region where a metal interconnect is connected to the upper electrode.